DEVELOPMENT OF DEVICES AND METHODS FOR PHASE AND AC LINEARITY MEASUREMENTS IN DIGITIZERS

U. Pogliano, B. Trinchera, G.C. Bosco and D. Serazio

INRIM – Istituto Nazionale di Ricerca Metrologica Torino (Italia)

Abstract

The present work, in the framework of the Task 2.4, was aimed at developing devices and methods for phase and ac linearity measurements in digitizers. In particular:

- a two-phase generator, able to generate suitable waveforms for characterizing measurement systems of precision ADCs;
- a wideband inductive divider for linearity characterization and phase of two phase digitizer;
- a program based on a commercial generator for the determination of the phase difference between a two phase digitizer and for the linearity of the phase shift in multitone signals.

The generator

The generator is based on an open platform commercial board, with high speed (1Gsamples/s for channel) and high resolution (16 bits). It is mainly intended to generate signals with a sharp time definition and, consequently, a good phase definition of the different harmonic components of the waveforms.

Different test functions are being implemented with this generator, as for example:

- sinusoidal signals with programmed characteristics (amplitude and phase) at the two outputs;
- multitone signal generation at the same output;
- signals with a programmed time jitter or phase shift variations.

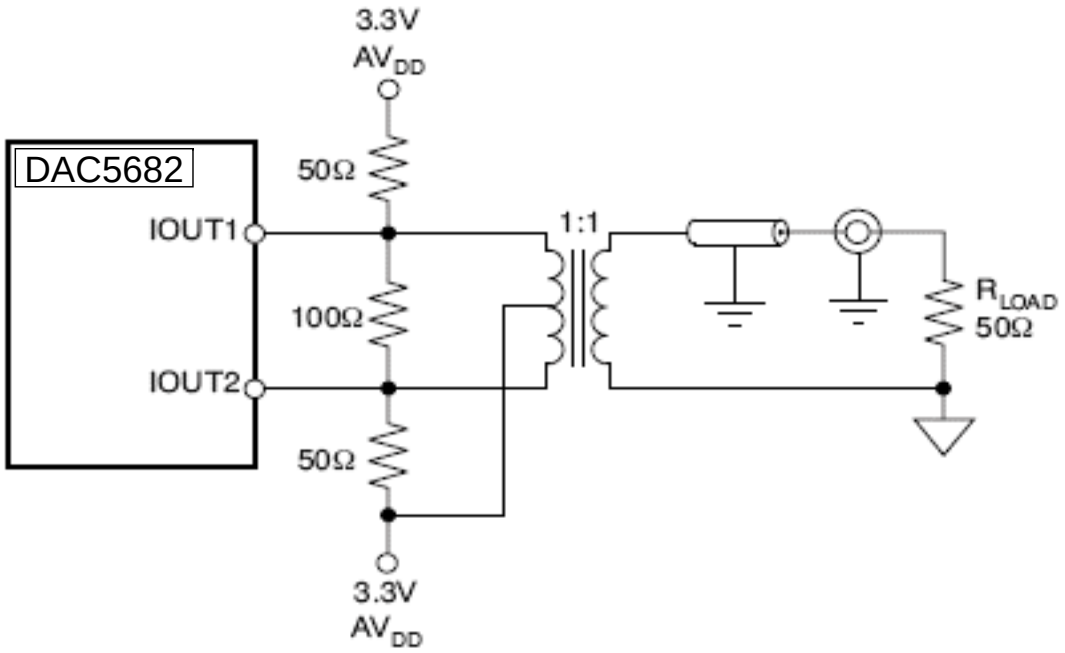
The generator is based on an open platform commercial board. There are two main blocks:

- a high performance field-programmable gate array (FPGA) board based on the VirtexV having 64 MB DDR2 SDRAM and 16 MB flash memory;
- an auxiliary board based on a double channels DAC and a high frequency phase-locked loop (PLL).

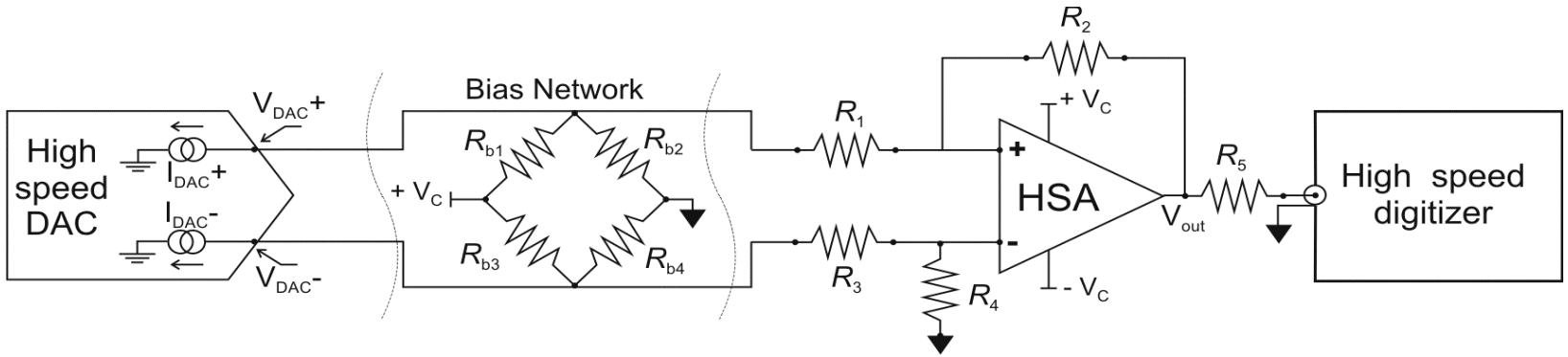
The high frequency clock is provided by a voltage controller crystal oscillator controlled by means of a high performance PLL clock synchronizer. FPGA makes possible the accurate synchronization of digital devices, by using internal distribute clock architecture.

Photo of the arbitrary open platform synthesizer, the high speed double output 1 Gsample/s DAC is mounted on a FPGA board based on Virtex5 device. The instrument requires no additional driver. The data can be sent or received by using a simple Windows application as the hyperterminal.

Output circuits

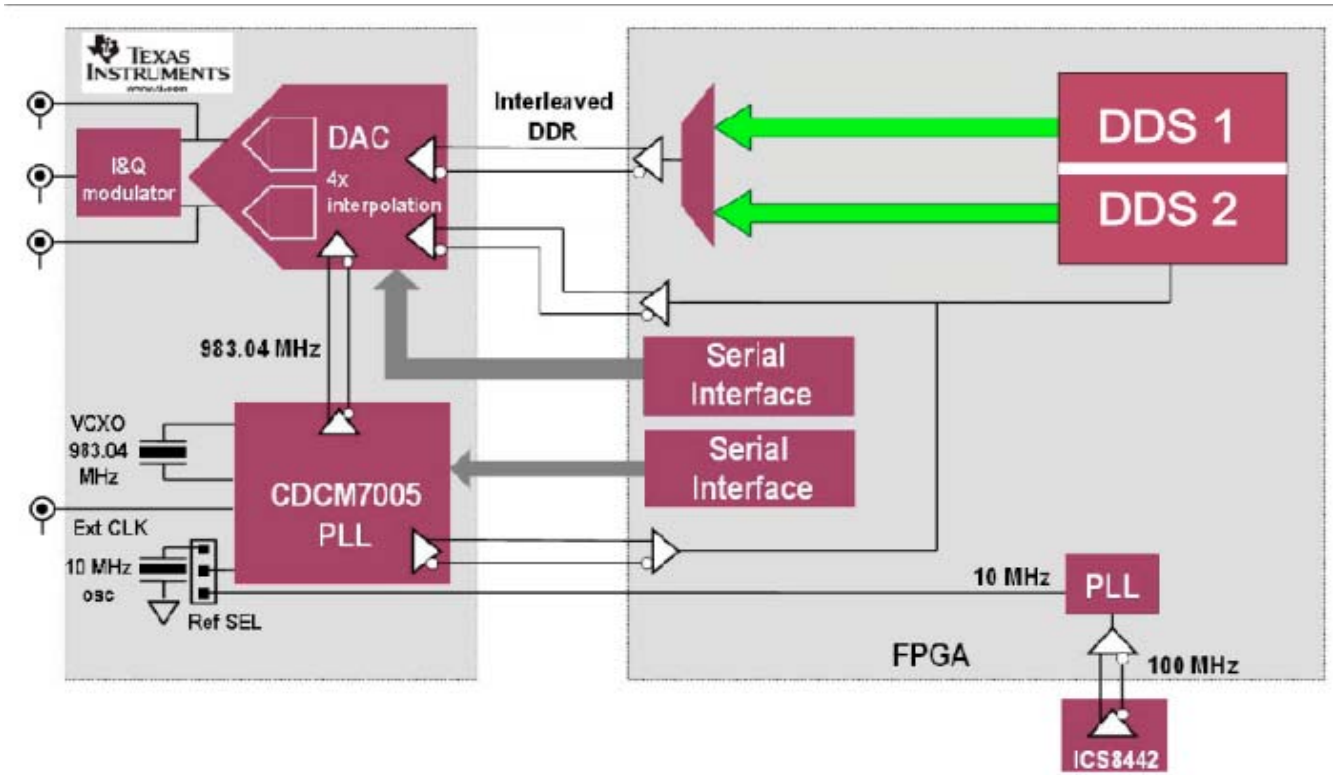


Originally the high speed DACs used for RF applications is configured to drive 50 Ω by a double terminated properly selected RF transformer, **which does not allows operation in dc and low frequencies.**



Modified output structure of a channel of the high speed DAC

Implementation of the DDS core multi generator



Input parameters

Direct digital synthesis (DDS) core compiler permits to set:

-The number of channels;

-System clock, up to 450 MHz;

-Spurious free dynamic range (SFDR);

-Frequency resolution;

-Memory type;

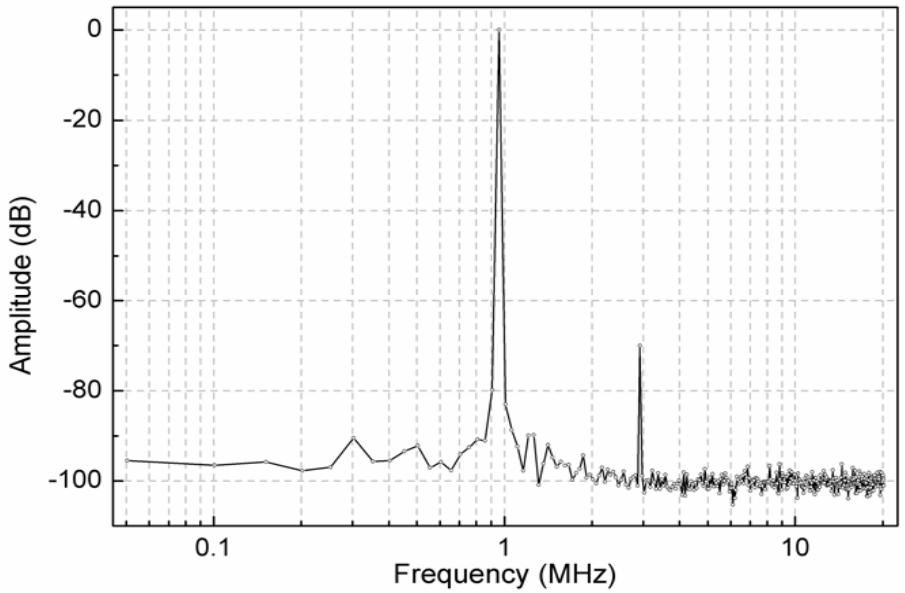
-Noise shaping (phase dithering algorithm);

-Latency.

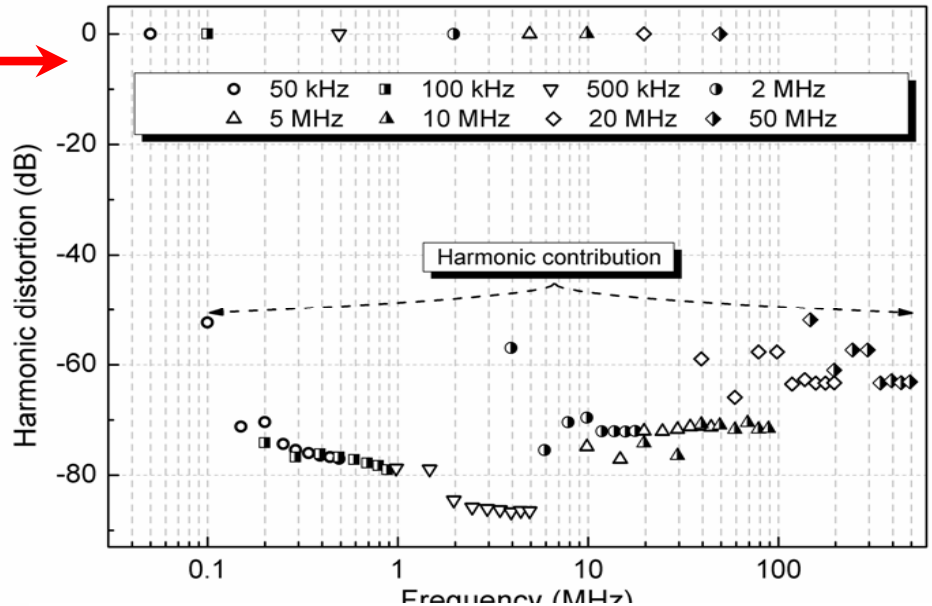
In these first tests each DDS module has 1 channel, system clock is 250 MHz, SFDR ≈ 96 dB and frequency resolution of 0.1 Hz. Each DDS core is described in VHDL (virtual hardware description language) and has separate programmable register (e.g. phase accumulator width of 32 bits for the frequency setting, and phase angle width of 14 bits for the phase offset setting).

Some tests on the generator prototype

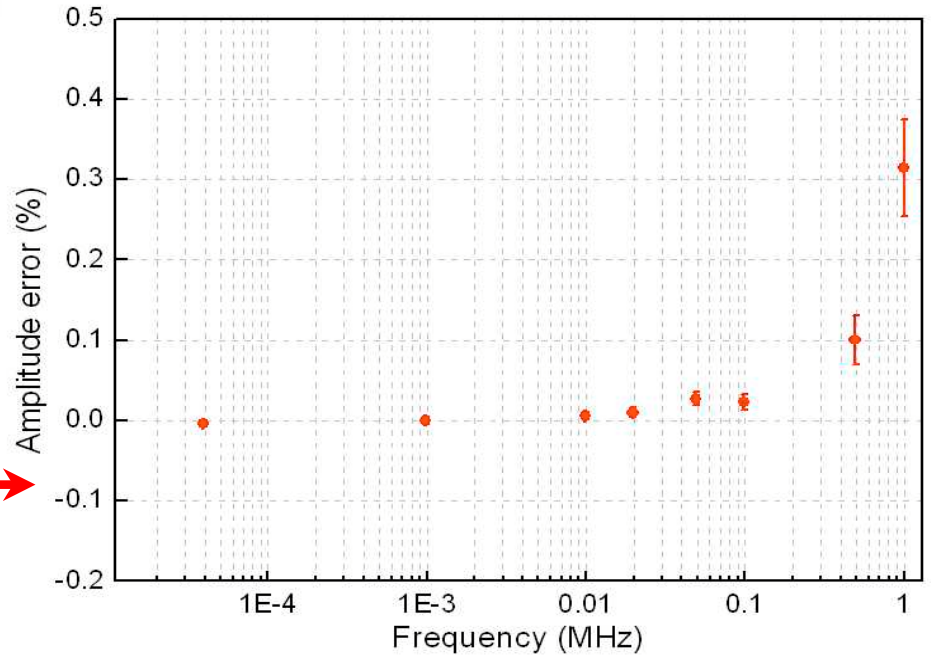
Harmonic contribution, up to ten, of ac single tones synthesized



Spectrum of a single tone of 1 MHz from 50 kHz to 20 MHz.

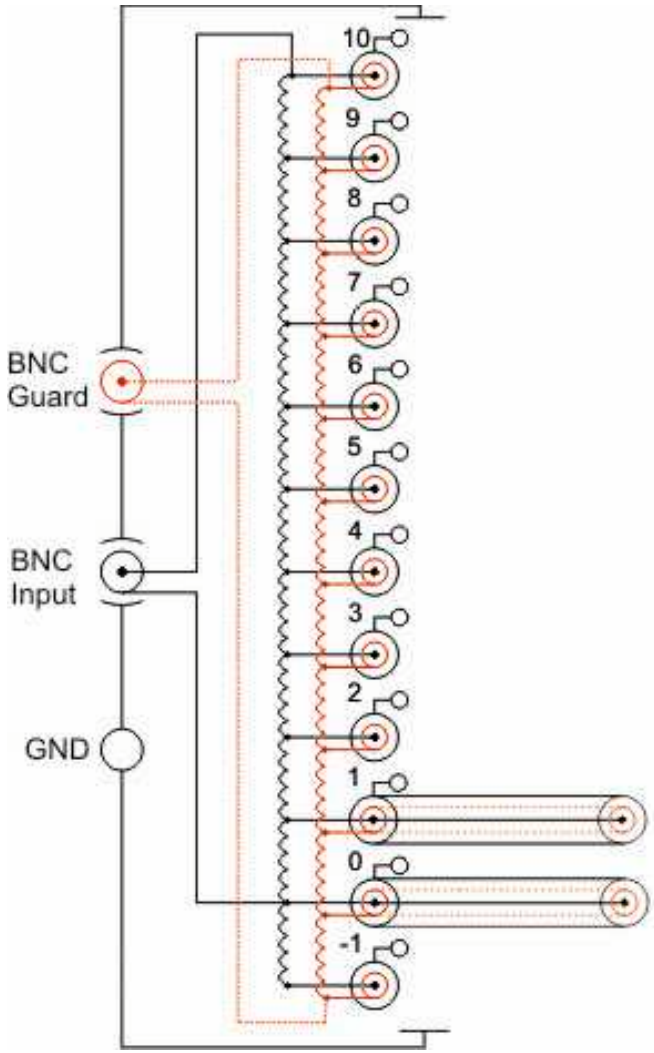


Amplitude relative error, measurements made with 20 cm of coaxial cable. The repeatability is about 45 ppm up to 1 MHz.

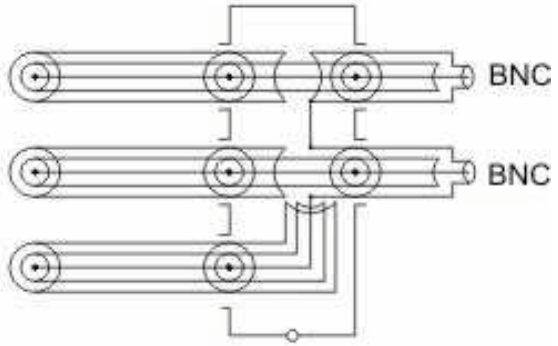


Wideband inductive divider

A modified version of wideband inductive divider with guard and cable connections has been build. The operative conditions are: voltage up to 10 V, frequency 500 Hz - 50 kHz.

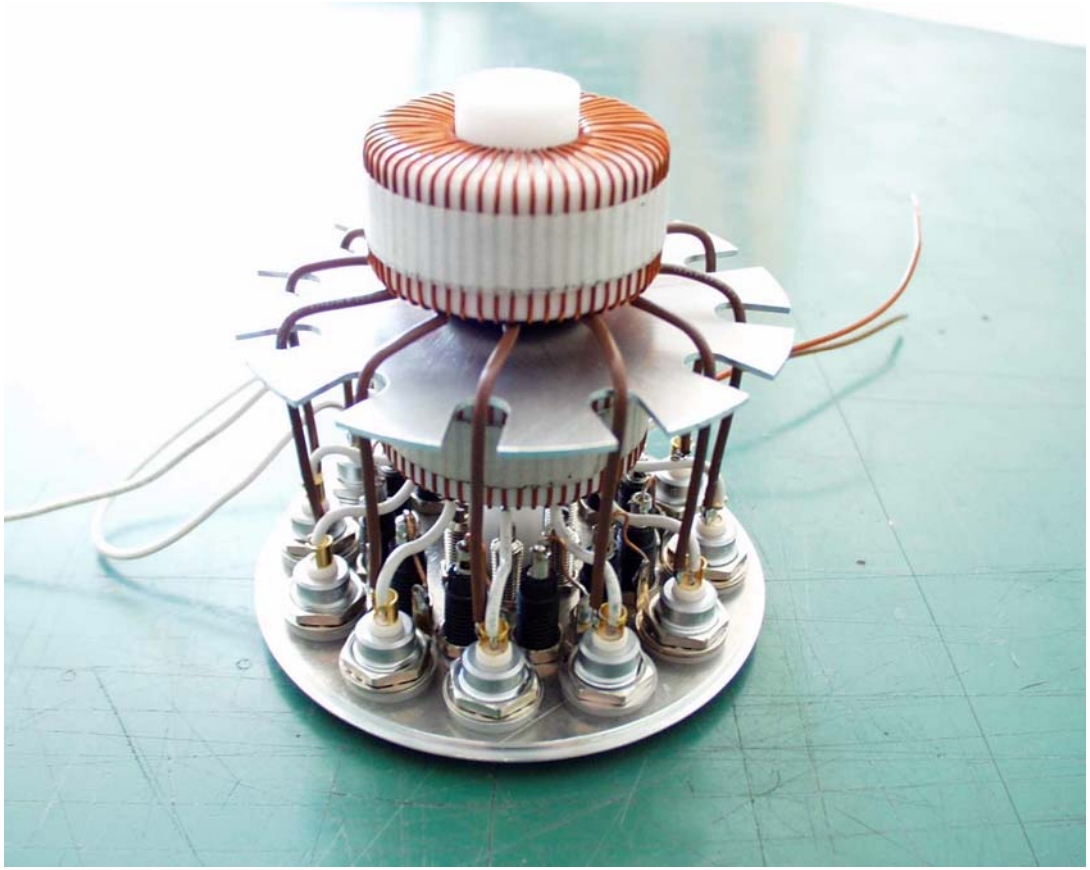


Scheme of the internal connections on the wideband inductive divider .

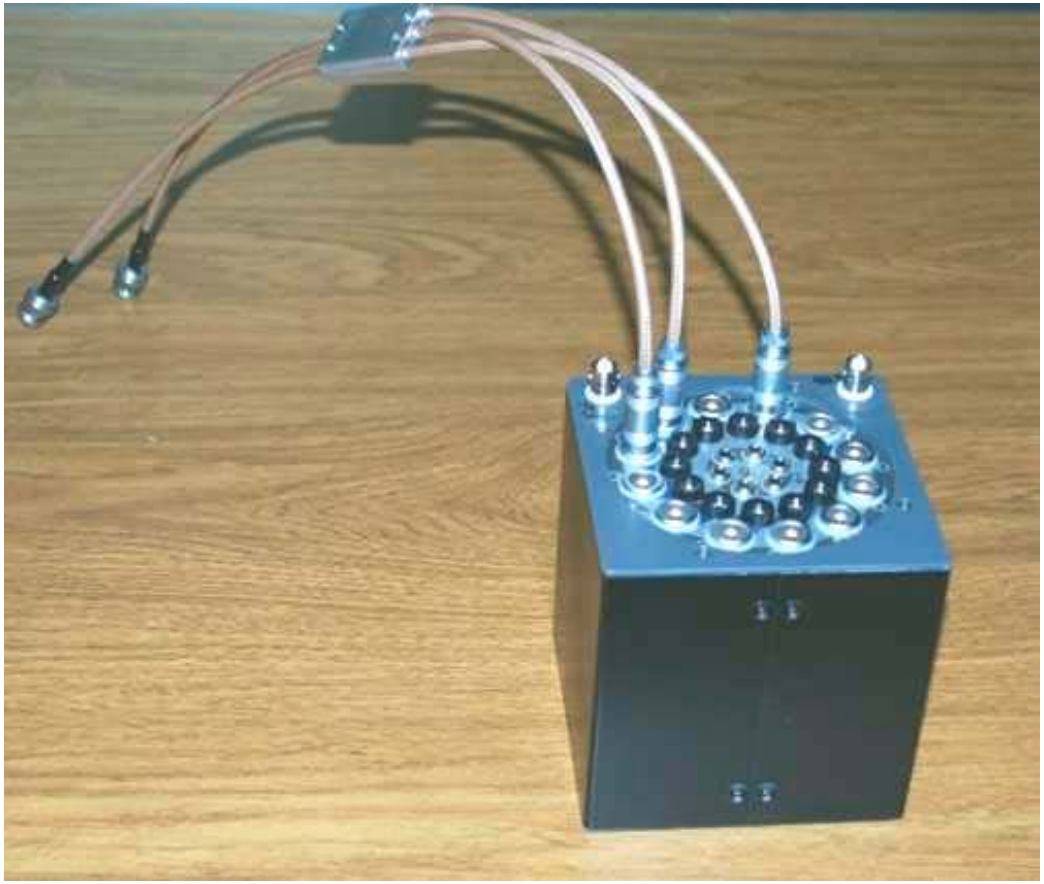


Scheme of the triaxial cables with guard for the connection to the two inputs of a digitizer.

Wideband inductive divider



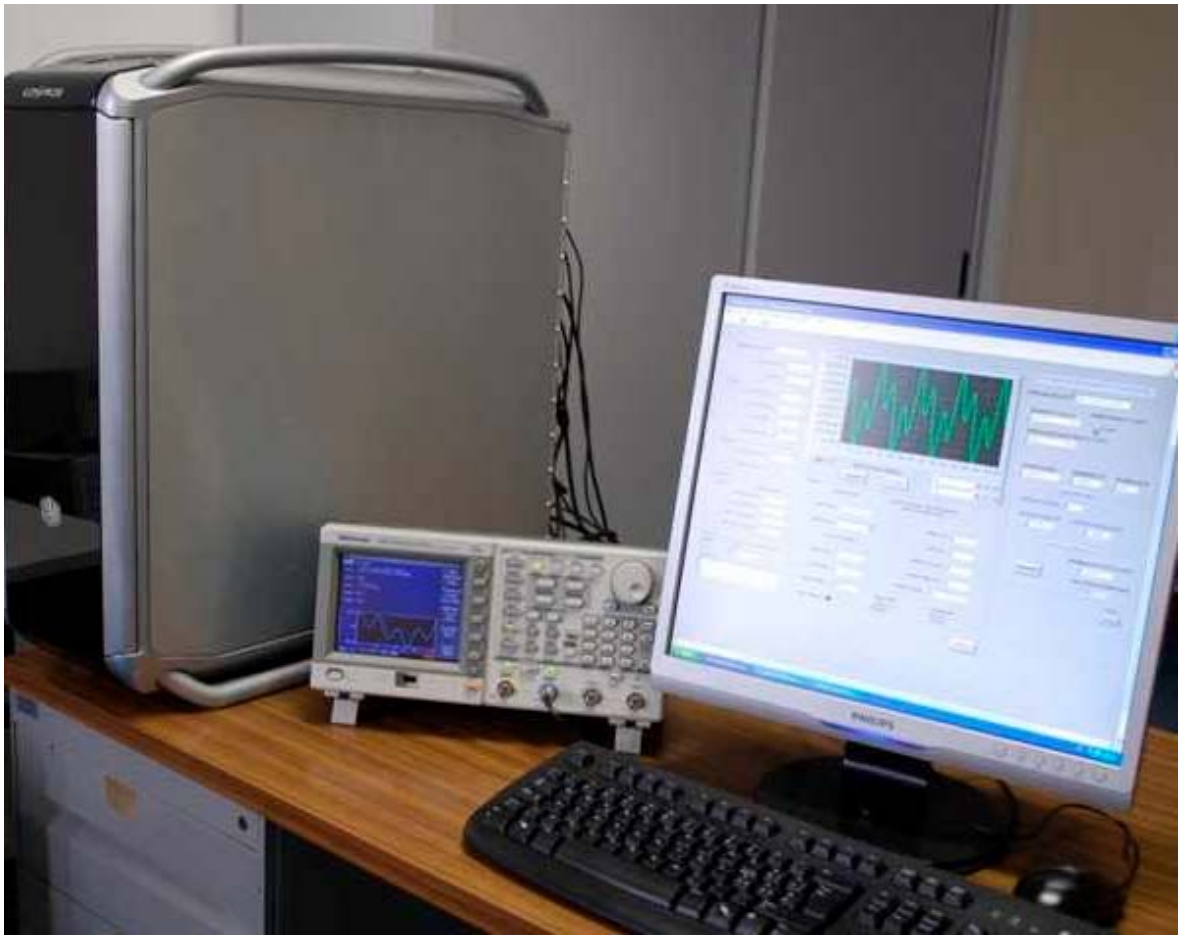
Internal connections of the main and auxiliary inductive dividers.



Wideband inductive divider with the cable connections.

Program for testing phase and phase shift

Two phase generator (Tektronik mod. AFG 3252) generation with look-up table mode (2 GS/s - 14 bits). Harmonic can be programmed for checking the linearity of the phase shift as function of the frequency. A Labview program has been develop to drive digitizer tests.



System for testing the digitizers in phase and in the linearity of the phase shift as function of the frequency.

The user interface allows the insertion of several configuration parameters of the digitizers (e.g. amplitude, sampling frequency, number of points, trigger, input decoupling…) and of the synthesizer (e.g. amplitude, phase and frequency of the fundamental and of the harmonic contents).